REMARKS

In this amendment, claims 23-30 are amended to more particularly point out the various embodiments of the invention. No new matter has been added as the amended subject matter is fully supported in the application as filed, and particularly in Fig. 2, as well as corresponding text of the Detailed Description.

Before addressing the claims, the Examiner's objections concerning the drawings and the specification (made in the Final Office Action dated July 2, 2003), are addressed. First, the Examiner states that no figures are provided showing how a charge is integrated or correlated double sampling is performed with respect to the blue pixels (where the blue reset shift register only has one reset bit in the embodiment described). However, directing now the Examiner's attention to the copy of Fig. 4 enclosed, reference letter AA points to the voltage wave form for blue pixels at row (n+1), where it is clear that the integration time TintB as indicated at the top of the figure jumps to its reset level at the point indicated by reference BB. No further figures are needed to describe to one of ordinary skill in the art how the charge is integrated or how correlated double sampling works, because the signal value for the blue pixel is read just before the voltage signal jumps to its reset value, and then the reset value is read.

The Examiner also objected to Fig. 4 as being apparently confusing. According to the Examiner, the timing for the red and green pixels is shown at *time* n and that for the blue pixels at *time* n+1. However, Applicants respectfully point out that the index n and n+1 does not refer to time but rather to different *rows* of the sensor array.

Finally, with respect to the Examiner's question as to how correlated double sampling can be performed for the blue pixel, using only one reset bit, Applicants provide the following explanation, which compares red and blue pixels. Note that in the copy of Fig. 4 attached to this amendment, the operation of red pixels is depicted by the sequence A-E, where operation begins with the first reset occurring as indicated by A. This reset causes the voltage for red pixels to jump to their reset value, and the start of integration occurs when the reset voltage drops, as indicated by B. Near the end of integration, a second reset is applied, as indicated at C. This in turn, causes the voltage of the red pixel to jump to its reset value as indicated at D. Note, however, that the

actual read-out of the voltage at the end of the integration time is enabled by the wordline signal, as indicated by the pulse at E. Thus, during the read enable pulse E, two values are read for the red pixel, namely the end-of-integration value, followed by the reset value. Similarly, two values are read for the blue pixel, enabled by the wordline signal at row (n+1).

In view of the foregoing discussion, it is submitted that the rejection of claims 26 and 30 under 35 U.S.C. §112, first paragraph, is also overcome as the specification clearly enables those of ordinary skill in the art to apply correlated double sampling using the architecture recited in claim 26, where a third reset shift register is recited that has only one reset bit. Accordingly, generating a pair of read bits is not critical or essential to the practice of the invention.

Finally, with respect to the art rejections, Applicants respectfully request that the Examiner reconsider the rejection in view of U.S. Patent 6,175,383 issued to Yadid-Pecht, et al. ("Yadid-Pecht") in view of others since these references do not teach or suggest the circuitry recited in claims 23 and 27 involving the color sensor array, and first and second reset shift registers and a wordline shift register, where the control logic is to program the reset bits of the pair of bits in each shift register to set the integration time independently for the first and second colors. The connection and use of such shift registers is not taught Yadid-Pecht because in Yadid-Pecht there are only wave forms described for controlling a pixel array without more.

CONCLUSION

In sum, a good faith attempt has been made to present claims that are submitted to be in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-

2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Dated: October 2, 2003

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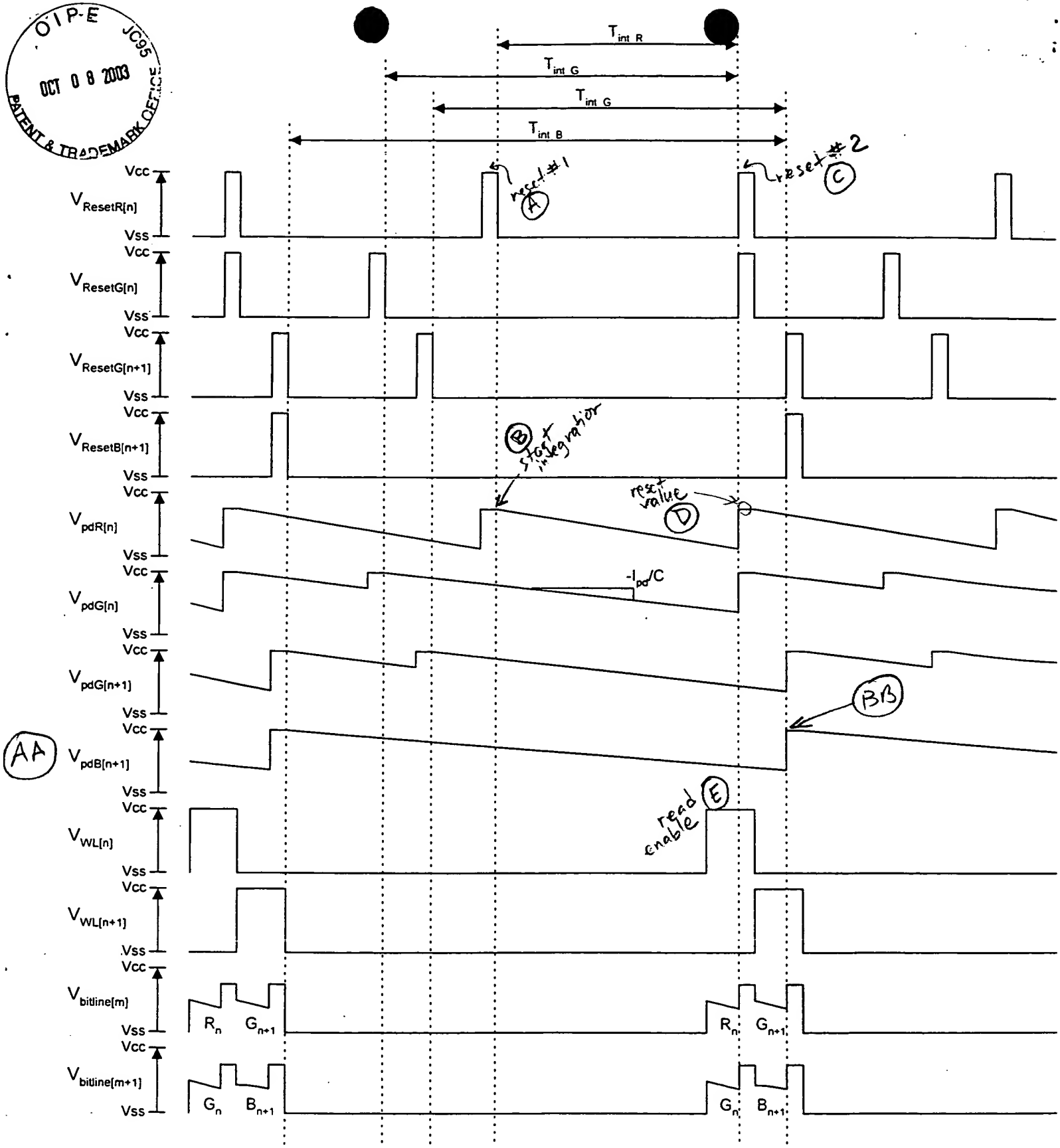
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on October 2, 2003.

Margaux Rodriguez October 2, 2003



COPY OF FIG. 4
FOR DISCUSSION ONLY